

With the buildout of 5G wireless networks and the constant demand for bandwidth in cloud-based data centers, serial link data rates continue to skyrocket. The current state-of-the-art serial links use ...

Since CTLEs are passive filters, they're no different in PAM4 systems than in PAM2-NRZ systems, but with four symbol levels, the decisions that PAM4 DFEs feedback are more complicated.

PAM4 effectively doubles the data rate for a link bandwidth at the expense of reduced signal to noise ratio (SNR). PAM4 is used in 400GE, 800GE, and 1.6T Ethernet as well as PCIe 6.0; and other ...

In this guide, we review the design considerations, associated challenges and solutions to the next generation of data center architecture built for 224G -- and how Molex matches solutions to ...

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800G switches have made significant leaps forward in data networking by leveraging 112G and 224G PAM4 SerDes technology. The 112G PAM4 SerDes is designed to transmit data at 112 gigabits per ...

These movements throughout the years have provided a baseline of traditional design goals that lead us to better understand today's 224 Gbps-PAM4 physical layer requirements.

This presentation intends to provide a 224 Gbps-PAM4 reference package model and parameter updates which are extracted from latest test/design packages for high radix switch and ASICs, as well as ...

Broadcom's Active Copper PHY portfolio enables DAC cable providers to build very low insertion-loss profile, ultra-low latency, ultra-low power cables for 100G/400G/800G/1.6T hyperscale/AI networks ...

This Pulse-Amplitude Modulation 4-Level (PAM4) application note explains PAM4 theory and operation while introducing the Intel's Stratix 10 TX device capability and the realization of 57.8 Gbps data ...

This application note explains PAM4 theory and its operation. It describes NRZ and PAM4 fundamentals, standards using PAM4 coding schemes, and CEI-56G Interconnect reaches and ...

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